A Very Low Cost and Highly Parallel DfT Method for Analog and Mixed-Signal Circuits

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***Abstract*—The quality level of the analog parts in mixed-signal ICs lags behind the below-part-per-million escape rates of the digital core. The reason is that analog blocks in these ICs have high test escape rates as a result of the typical testing based on performance specifications. Test point selection/insertion techniques have been proposed to solve this problem by offering increased observability. However, their effectiveness in practice is still limited due to the lack of a commonly accepted methodology to make probing of internal nodes in analog circuitry possible. This paper presents a low-cost and highly parallel DfT technique based on inserting testing diodes to internal circuit nodes, which enables those test point selection algorithms at low cost. An industrial case study demonstrates 90.4% fault coverage value with a very small overhead in area and test time.**

I. Introduction

The quality levels of typical mixed-signal ICs are predominantly decided by the analog circuitry, although the major part of the area comprises the digital core. The reason is that the digital part is tested by well-defined structural tests for more than decades, whereas the analog blocks are traditionally tested according to functional specifications. This empirical approach results in long and expensive test sets which cause analog testing to dominate the testing effort and cost for mixed-signal ICs. Furthermore, these specification-based tests often lead to poor fault coverage for the analog circuits, since the possible defects are not directly addressed in such a methodology [1].

In order to improve the analog fault coverage, previous works have focused on test point selection/insertion algorithms [2] [3]. These studies are based, mostly, on the selection of the list of internal nodes that need be probed in an analog circuit to offer increased observability.

However, no commonly accepted DfT technique has been presented which can enable these test point selection/insertion methodologies in practice and satisfy the specific requirements of low area overhead, short test time, being non-intrusive, etc. Early DfT work has concentrated on using analog voltage buffers to probe out internal nodes in a similar manner to the scan chain for digital circuits [4]. The evident disadvantages of this methodology are the large area overhead and the long testing time because of the serial manner of testing. The loading effect introduced by analog voltage buffers also makes this approach almost inapplicable to many analog circuits. Current-based probing has been adopted to overcome the problem of excessive loading. However, this technique also suffers from large area overhead and long testing time [5]. A low-cost analog test bus has been introduced that significantly decreases the area overhead and the loading effects [6]. Nevertheless, this technique also requires impractically long test times, because of the lack of parallelism.

In this paper, a novel DfT technique is proposed based on using testing diodes to probe out the DC values of internal nodes in a parallel manner [7]. The proposed DfT technique has the following advantages:

- a very small area overhead which is dominated by the routing and therefore can further be optimized;
- a small capacitive loading on the selected nodes, which ensures an almost non-intrusive normal operation;
- a high level of parallelism which results in a short test time.

The paper is organized as follows. In Section II, the proposed approach will be explained in detail. In Section III, a case study will be presented which demonstrates the effectiveness of the proposed method on industrial circuits. Conclusions will be drawn in Section IV.

II. Proposed DfT Method

Defects in analog circuits are not always detectable by only inspecting primary outputs because of the inherent complexity of analog circuits and the process variations. Detecting those hard to cover defects certainly requires improving the observability and/or the controllability of the internal nodes. A novel DfT technique is proposed which enables internal nodes to be tested for defects in order to improve the analog fault coverage. Fig. 1 illustrates two different configurations of the proposed method, which encompasses adding testing diodes and assigned test pins, to the circuit under test (CUT).

There are two possible configurations of the proposed technique for every voltage domain in the circuit, since there are two types of possible faults which can be detected in this way. The first one is called a pull-down fault and can be defined as a fault representing a defect that tends to pull the DC operating voltage of a node lower than designed. The second type is called a pull-up fault and represents a defect which has the opposite effect. A voltage domain is a group of nodes that operates within the same DC voltage range. Any analog integrated circuit can be divided into a number of voltage domains by defining a certain voltage range for each of them. For the proposed method, the threshold voltage of a diode limits and also defines the maximum range for every voltage domain that is to be tested from one test pin. In any case, the defined range of the voltage domains should

be smaller than the possible change caused by a pull-up or a pull-down fault.

The configuration shown in Fig. 1 is comprised of testing diodes which enable or disable current flowing through the test pin controlled by the applied test voltage, i.e. V_{D1} and V_{D2}. It should be noted that all anodes of the diodes are connected together for the first voltage domain, so that the pull-up type of faults can be detected. During normal operation of the circuit, the voltage applied to the test pin, i.e. V_{D1}, is pulled up (connected to the supply voltage) such that unconditional reverse biasing of all testing diodes is assured and the circuit is not disturbed. In the test mode, a predefined test voltage, which is calculated such that the testing diodes do not conduct current for the defect-free circuit, is applied to the test pin. In other words, the voltage difference between the normal operating voltage of the concerned internal nodes (N1, N2 and N3) and the test voltage does not exceed the threshold voltage of the diode, therefore no current flows. Since the testing diodes remain closed for the defect-free circuit, a very small loading effect is applied to the circuit even in the test mode.

In case of a pull-up fault influencing the related nodes, one of the testing diodes will conduct some current, which can readily be detected from the test pin as an indication of the defective circuit. For instance, in the case of a fault affecting the node N1, the voltage at this node will be higher than its designed value. When the test pin, therefore the cathode of the diode, is pulled down to the predefined level during the test mode, this will create enough difference for the related diode to be forward biased. The resulting current is then detected through the test pin. In the case of a fault affecting the node N2, the voltage at this node will be higher than its designed value which is supposed to be in the same voltage domain with node N1. Therefore, in the test mode, the related diode will be conducting, which can also be detected in parallel from the same test pin. Pull-down faults influencing nodes N4, N5 and N6 can be detected in a similar manner by using the other configuration shown Fig. 1.

III. Case Study

An industrial trimmable op-amp circuit, which includes 40 transistors, is used as a case study for two reasons. First of all, it is a very common and generic building block for analog and mixed-signal ICs. The other reason is the limited controllability and observability of the input and output terminals of the block inside large-scale ICs. Since it is not practical to assign separate test pins to every op-amp in an IC, the common way of testing these blocks is to probe each output, in a serial manner, through an analog test bus. This, in return, is very time consuming and highly dependent on the accuracy of the analog switches.

Fault simulations have been carried out for the industrial trimmable op-amp test case. Test point selection has been implemented using these fault simulations in order to determine those internal nodes which are to be used by the proposed method. The selection of these nodes is not in the scope of this work, since several test point selection algorithms have been presented by earlier publications. A fault coverage of 90.4% is achieved by introducing only two testing diodes to the internal nodes according to the proposed DfT approach, without any other accessibility. The required extra area to add these diodes is negligible compared to the area of the op-amp circuit.

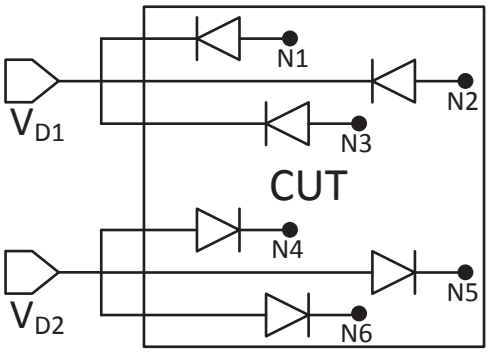

Fig. 1. Block diagram of the proposed method with two different configurations for pull-up and pull-down cases.

IV. Conclusion

A very low cost DfT technique, which involves connecting testing diodes to internal nodes of an analog circuit, has been introduced. The high level of parallelism of the proposed technique is very effective in terms of test time. Furthermore, the area overhead is negligible and routing dominated, which can be further optimized.

An industrial case study has shown a 90.4% fault coverage with a negligible area overhead and a short test time. Besides, each testing diode adds only negligible parasitic capacitive loading to the internal nodes.

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